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09/668,109	09/22/2000	Steven J. Meyer	2470.01US02	9581

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EXAMINER

CHANG, SUNRAY

ART UNIT	PAPER NUMBER
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2121

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,109	MEYER, STEVEN J.	
	Examiner	Art Unit	
	Sunray Chang	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-5, 9-12, 16-20, and 22-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in responsive to the paper filed on August 23, 2004.
2. Claims 2 – 5, 9 – 12, 16 – 20, and 22 – 24 are presented for examination.
Claims 1, 6 – 8, 13 – 15, and 21 are canceled.
Claims 2 – 5, 9 – 12, 16 – 20, and 22 – 24 are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
-
3. **Claims 2 – 5, 9 – 12, 16 – 20, and 22 – 24 are rejected** under 35 U.S.C. 103(a) as being unpatentable over William C. Steinmetz Jr. (U.S. Patent No. 5,600,579 and referred to as

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Steinmetz hereinafter), and in view of Lansing Dunn Pickup (U.S. Patent No. 5,774,380, and referred to as Pickup hereinafter).

(Steinmetz as set forth above generally discloses the basic inventions.)

Regarding Claim 22 – 24, Steinmetz teaches,

- Electronic circuit model portions have been coded into a hardware description language (HDL). [Master model is coded in the Verilog HDL language, Col. 2, Line 5]
- A processor [CPU, Col. 1, Line 45] having memory [emulated ^ememory device, Col. 1, Line 49] for storing a program that is capable of being executed by said processor [instructions, loaded into memory, Col. 1, Line 54 – 56].
- Convert each of the HDL coded electronic circuit model portions [compiling the master model computer program to produce the master model, Col. 28, Line 58 – 59] to a binary object code [object code, Col. 28, Line 61].

Steinmetz does not teach, a simulator-independent, model compiler system for compiling an electronic circuit model, at least one portion is different from another portion, each binary code utilizes a similarly configured simulator-independent binary object code sequence instead of the HDL, enable simulator-independent object code to make calls to a programming language interface (PLI) of a simulator.

Pickup teaches,

- A simulator-independent [allow this data to be used in other simulation scenarios, Col. 1, Line 12 – 13] model compiler system for compiling an electronic circuit model [Col. 1, Line 10 – 13].
- One portion [user defined primitive, Col. 2, Line 40] is different from other portion [sequential devices, Col. 2, Line 36].
- Each binary code utilizes a similarly configured simulator-independent binary object code sequence [Col. 2, Line 35 – 37].
- Enable simulator-independent object code to make calls [initialize, Col. 2, Line 38] to a programming language interface (PLI) of a simulator [another simulation scenario, Col. 2, Line 38].

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Steinmetz to include "a simulator-independent, model compiler system for compiling an electronic circuit model, at least one portion is different from another portion, each binary code utilizes a similarly configured simulator-independent binary object code sequence instead of the HDL, enable simulator-independent object code to make calls to a programming language interface (PLI) of a simulator." for the purpose of reducing scenario execution time.

4. **Regarding dependent claim 2**, Steinmetz teaches program (test script, Col 28, Line 51) directs (steps, Col 28, Line 41) said processor (computer, Col 27, Line 32) to convert (coupled, Col 3, Line 8) the HDL coded electronic circuit model portions (master model, Col 3, Line 8) to

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binary object code (object code, Col 28, Line 61) by directing (steps, Col 28, Line 41) said processor (computer, Col 27, Line 32) to translate (coupled, Col 3, Line 8) the HDL coded electronic circuit model portions (master model, Col 3, Line 8) into an intermediate program language code (master model computer program, Col 28, Line 58) and to compile (compiling, Col 28, Line 58) said intermediate program language code (master model computer program, Col 28, Line 58) to said binary object code (object code, Col 28, Line 61).

5. **Regarding dependent claims 3, 10 and 18**, Steinmetz teaches intermediate program language code (master model computer program by means of PLI, Col 12, Line 17) is a C program language code (C programming language, Col 2, Line 24).

6. **Regarding dependent claims 4, 11 and 19**, Steinmetz teaches C program language code (PLI program, 2, 24) is grouped into code types selected from a group consisting of: evaluation C code (functionally, Col 1, Line 46) and scheduling C code (correctly timed, Col 1, Line 46).

7. **Regarding dependent claims 5, 12 and 20**, Steinmetz teaches binary object code (object code, Col 28, Line 61) performs operations that are selected from a group consisting of: initial/always block operations (block diagram, Fig. 1, 3), timing-free procedural operations (reading data from memory, Col 2, Line 11), task procedural operations (multitasking operating, Col 5, Line 16), function procedural operations reading data from memory, Col 2, Line 11), event control operations (event handling, Col 19, Line 34), delay control operations (set simulation timing, Col 22, Line 25), scheduled procedural operations (set simulation timing, Col

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22, Line 25), declarative gate operations (get level model, Col 1, Line 44), continuous assignment operations (get level model, Col 1, Line 44), user-defined primitive operations (defined by user, Col 6, Line 27), delay path operations (manipulate wire, Col 22, Line 23), system task operations (multitasking operation, Col 5, Line 16), and system service operations (operating system, Col 3, Line 23).

Dependent claims 5, 12 and 20 are drawing to operations such as "block operation", "procedural operation", "event control", "task operation", etc those are inherent in hardware simulators. Examples disclosed by Steinmetz showed above.

8. Regarding dependent claims 9 and 17, Steinmetz teaches the steps of translating (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) into an intermediate program language code (master model computer program, Col 28, Line 58) and compiling (compiling, Col 28, Line 58) the intermediate program language code (master model computer program, Col 28, Line 58) to said linkable simulation program (object code, Col 28, Line 61).

9. Regarding dependent claim 16, Steinmetz teaches simulator (verification system, Col 28, Line 55) -operable (functions, Col 28, Line 56) program comprises binary object code (object code, Col 28, Line 54).

Response to Amendment

Claim Rejections - 35 USC § 112

10. The amendment overcomes 112-second paragraph rejection “as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention” by changing the “function” to “function procedural operation” [Page 6, line 1] in the specification, reasonably pointing out the subject matter. Examiner has withdrawn the rejection.

11. The amendment overcomes 112-second paragraph rejection “implicit wired operations in claims 5, 12, and 20 are vague and indefinite” by adding the “implicit wire operations” [Page 23, line 10] in the specification, reasonably pointing out the subject matter. Examiner has withdrawn the rejection.

12. The amendment overcomes 112-second paragraph rejection “The term function procedural operations in claims 5, 12, and 20 is vague and indefinite” by changing the “function” to “function procedural operation” [Page 6, line 1] in the specification, reasonably pointing out the subject matter. Examiner has withdrawn the rejection.

Claim Interpretation

13. The claim interpretations were based on 112-second rejections, since the amendment overcomes 112-second rejections. Examiner has withdrawn the claim interpretations.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is 571-272-3682. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571)272-3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-746-3506.

Sunray Chang
Patent Examiner
Group Art Unit 2121
Technology Center 2100
U.S. Patent and Trademark Office

August 23, 2004



Anthony Knight
Supervisory Patent Examiner
Group 3600